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FOR

SIMPLIFIED COMPARATOR WITH DIGITALLY CONTROLLABLE HYSTERESIS AND BANDWIDTH

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SIMPLIFIED COMPARATOR WITH DIGITALLY CONTROLLABLE HYSTERESIS AND BANDWIDTH

FIELD OF THE INVENTION

[0001] The present invention relates to the field of electronic circuits. More specifically, the present invention relates to comparator electronic devices.

BACKGROUND

[0002] Integrated circuit ("IC") chips are becoming more densely packed with millions of electronic components. In order to manufacture various IC chips for specific applications, new technologies have been developed to satisfy the requirements of these chips. Each technology typically requires a set of specifications, such as voltage and frequency requirements. With the increasing number of semiconductor technologies in recent years, industries and/or IEEE have adopted various standards to facilitate communications between various chips. For example, when multiple chips are mounted on a printed circuit board ("PCB"), it is critical to understand what standard each chip follows so that they can properly communicate with each other. However, with the increasing number of standards on a single PCB, testing a PCB with various IC chips becomes more difficult.

[0003] A conventional test mechanism used in the past for testing a PCB is the boundary-scan testing. For example, IEEE 1149.1 supports testing of interconnections between IC pins. Scan test is typically performed by various scan circuits, also known as scan cells. Scan cells are usually located at the edge of the chip and they typically only perform testing functions. As such, it is advantageous to design scan cells as efficiently as possible because they don't typically contribute to the general functions of the chip. Scan cells generally include various comparators, which may be used to receive and to identify input signals.

[0004] Comparators are widely used in a variety of electronic equipment to compare the voltages of two analog inputs and to provide a digital output. A conventional comparator is an amplifier with a positive and a negative input, which typically has high input impedance. A comparator usually has high gain and produces an output signal that is the amplified difference of the positive and negative input signals. In general, a conventional comparator can be used to determine if an input signal is logically above or below a reference voltage. To enhance the noise immunity for the comparator, a technique of using hysteresis is often employed to reduce the effect of noise.

[0005] A hysteresis threshold typically defines the difference between "no input" and "input." The terms of hysteresis threshold, hysteresis offset, hysteresis offset voltage, and/or hysteresis voltage can be used interchangeably herein. A hysteresis comparator typically switches its output to one output state when the input is above one level and switches to the opposite output state when the input is below a lower level, and the output does not switch at any intermediate level.

[0006] **Figure 1** shows a schematic diagram of a conventional comparator 100 having a hysteresis offset voltage. Comparator 100 includes a comparing circuit 104 and an element 102, which generates a hysteresis offset V_{hyst}. The use of hysteresis can reduce an unwanted response to small signal noise. Typically, comparing circuit 104 outputs an output signal in response to input signals at input terminal In1-In2 and a hysteresis offset which is provided by element 102.

[0007] **Figure 2** is a schematic diagram of a device 200 for a conventional method of creating a hysteresis offset voltage. Device 200 includes two identical n- or n-type transistors N3-4, resistors R1-2, and current sources S3-4. If the values of transistors, resistors, and current sources are properly sized, a desirable hysteresis offset can be created across the resistor R2. Once the hysteresis offset is created, the device 200 may discard

some small input signals at terminals 206-208 according to the value of the hysteresis offset.

[0008] A problem with the conventional hysteresis comparator is that it takes too many components, such as two transistors, two resistors and two current sources, to generate a hysteresis offset. Another problem with the conventional hysteresis comparator is that it is difficult to adapt new and/or different standards because each standard may require a different hysteresis offset or hysteresis delay.

[0009] Thus, it would be desirable to have a comparator that is capable of generating selectable hysteresis offsets and hysteresis delays.

SUMMARY OF THE INVENTION

[0010] A programmable comparator capable of producing a digital signal in response to differential input signals is disclosed. In one embodiment, the programmable comparator includes a programmable hysteresis offset circuit, which is configured to selectively provide a hysteresis offset in response to a programmable hysteresis offset control signal. The programmable comparator further includes a comparing circuit, which is capable of receiving differential signals through input terminals and outputting a digital signal via an output terminal. In one embodiment, a user can select a hysteresis offset to enhance the noise immunity.

[0011] In another embodiment, the programmable comparator includes a programmable hysteresis delay circuit that is operable to selectively provide a hysteresis delay in response to a programmable hysteresis delay control signal. The comparing circuit is capable of outputting digital information in response to the differential input signals and the hysteresis delay. In this embodiment, a user can select a hysteresis delay out of multiple possible hysteresis delays to increase the noise immunity.

[0012] In another embodiment, a first input transistor includes a first terminal, a second terminal and a gate terminal. The gate terminal of the first input transistor is connected to a first input and the first terminal of the first input transistor is electrically connected to a first reference voltage via a first electrical path. The first electrical path includes a current source and a resistor to generate a hysteresis offset. A second input transistor has a first terminal, a second terminal and a gate terminal. The gate terminal of the second input transistor is connected to a second input and the first terminal of the second input transistor is electrically connected to the first reference voltage via a second electrical path. The first electrical path including a current source. An output is capable of being pulled toward the first reference voltage or a second reference voltage depending in part whether the hysteresis offset has been exceeded.

[0013] Additional features and benefits of the present invention will become apparent from the detailed description, figures and claims set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The present invention will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the invention, which, however, should not be taken to limit the invention to the specific embodiments, but are for explanation and understanding only.

[0015] **Figure 1** shows a schematic diagram of a conventional comparator having a hysteresis offset voltage;

[0016] **Figure 2** is a schematic diagram of a device for a conventional method of creating a hysteresis offset voltage;

[0017] **Figure 3A and 3B** are timing diagrams illustrating digital output waveforms in response to mixed signal input waveforms in accordance with one embodiment of the present invention;

[0018] **Figure 4** is a schematic diagram illustrating an implementation of a hysteresis comparator in accordance with one embodiment of the present invention;

[0019] **Figure 5** is a schematic diagram illustrating a comparator capable of receiving input signals in response to a hysteresis offset and a hysteresis delay in accordance with one embodiment of the present invention;

[0020] **Figure 6** is a block diagram illustrating a hysteresis comparator capable of receiving input signals in response to a programmable hysteresis offset and a programmable hysteresis delay in accordance with one embodiment of the present invention;

[0021] **Figure 7** is a block diagram illustrating a programmable comparator having a resistance component in accordance with one embodiment of the present invention;

[0022] **Figure 8** is a detailed circuit diagram illustrating a comparator having multiple programmable blocks in accordance with one embodiment of the present invention;

[0023] **Figure 9** is a schematic diagram illustrating a comparator having detailed programmable circuits in accordance with one embodiment of the present invention;

[0024] **Figure 10** is a block diagram illustrating a fixed signal comparator for boundary-scan testing in accordance with one embodiment of the present invention;

[0025] **Figure 11** is a flow chart illustrating a scheme of producing a digital output signal according to mixed input signals in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0026] A method and apparatus of a programmable comparator capable of outputting a digital signal in response to differential input signals and programmable hysteresis references are disclosed. In one aspect, hysteresis references include a hysteresis offset and a hysteresis delay. In the following description, for purposes of explanation, numerous specific details are set forth to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that these specific details may not be required to practice the present invention. In other instances, well-known circuits and devices are shown in block diagram form to avoid obscuring the present invention.

[0027] It is understood that the present invention may contain transistor circuits that are readily manufacturable using well-known art, such as for example CMOS ("complementary metal-oxide semiconductor") technology, or other semiconductor manufacturing processes. In addition, the present invention may be implemented with other manufacturing processes for making digital and system devices.

[0028] In the following description of the embodiments, substantially the same parts are denoted by the same reference numerals.

[0029] The present invention discloses a method and an apparatus of a programmable comparator that is capable of producing a digital output signal in response to differential input signals with adjustable and/or user programmable hysteresis information. The programmable comparator includes a programmable hysteresis offset circuit. The comparator produces an output signal that is the amplified difference of the input signals. A comparator, in one aspect, can be used as a differential receiver to determine if an input signal is logically above or below a reference voltage. In one embodiment, the programmable hysteresis offset circuit selectively provides a hysteresis offset according to the hysteresis offset control signal. The terms hysteresis offset,

hysteresis voltage, hysteresis reference voltage, and hysteresis threshold can be used interchangeably herein.

[0030] **Figure 3A** is a timing diagram 300 illustrating a digital output waveform in response to a mixed signal in accordance with one embodiment of the present invention. Mixed signals, in one embodiment, include digital and analog signals. Timing diagram 300 includes an input signal (waveform) 302 and an output signal (waveform) 306. Input signal 302 may include digital pulses, analog pulses (not shown in Figure 3A), and intermittent noise pulses 340-342. In one embodiment, output signal 306 is always in digital waveform regardless of whether the input signal contains digital and/or analog pulses.

[0031] Timing diagram 300 shows a hysteresis offset 332 and hysteresis delay 330. As mentioned earlier, the use of hysteresis offset 332 is to reduce an unwanted response to small signals generated by noise. The use of hysteresis delay 330 is to reduce noise effects from voltage spikes. In other words, the utilization of hysteresis offset 332 causes the comparator to ignore small-amplitude pulses with sufficient duration while the utilization of hysteresis delay 330 causes the comparator to disregard large-amplitude pulses with insufficient duration.

[0032] Referring to **Figure 3A**, at time 310, input signal 302 starts to rise. Input signal 302 reaches the voltage of hysteresis offset 332 at time 311. At time 313, output signal 306 starts to respond to input signal 302 after the pulse of input signal 302 sustains as long as hysteresis delay 330. At time 312, output signal 306 starts to fall in response to the fall of input signal 302. At time 314, a voltage spike 340 appears at input signal 302 but it fails to affect output signal 306 because the duration of the spike 340 is not long enough. At time 316, a noise pulse 342 appears at input signal 302 and it also fails to affect the output signal 306 because it does not have enough voltage amplitude.

[0033] The timing diagram 300 shown in **Figure 3A** illustrates an example of a comparator, which employs a hysteresis offset for reducing the effect of small-amplitude noise and uses a hysteresis delay for reducing the effect of large-amplitude pulses of insufficient duration.

[0034] **Figure 3B** is a timing diagram 350 illustrating a digital output waveform in response to an analog signal in accordance with one embodiment of the present invention. It should be noted that the input signal may also be a mixed signal and/or digital signal. Referring to **Figure 3B**, timing diagram 350 includes an input signal (waveform) 352 and an output signal (waveform) 356. Input signal 352, in one embodiment, includes analog pulses 351-352 and intermittent noise pulses 380-382. Timing diagram 350 shows a hysteresis offset 372 and hysteresis delay 370. As mentioned earlier, the use of hysteresis offset 372 is to reduce an unwanted response to small signals generated by noise. The use of hysteresis delay 370 is to reduce noise effects from voltage spikes.

[0035] In one embodiment, output signal 356 is always in digital waveform even though the input signals are analog pulses. For an AC coupled receiver, positive analog pulse triggers the rising edge of the digital output signal and negative analog pulse triggers the falling edge of the digital output signal. In another embodiment, a first analog signal triggers the rising edge of the digital output signal and a second analog signal triggers the falling edge of the digital output signal. In one embodiment, output signal 356 changes its digital waveform in response to analog input signals, which are typically in a range between 50 and 300 millivolts (mV).

[0036] Referring to **Figure 3B**, at time 360, input signal 352 starts to rise. Input signal 352 reaches the voltage of hysteresis offset 372 at time 361. At time 362, output signal 356 starts to respond to input signal 352 after the pulse 351of input signal 352 sustains as long as hysteresis delay 370. As mentioned earlier, for an AC coupled device, a positive analog pulse 351 triggers the rising edge of the digital output signal 374. Once the

output signal 356 reaches high state 376, it stays high until the next analog pulse. At time 366, output signal 356 starts to change its waveform (a falling transition) in response to a negative analog pulse 352 of input signal 352. At time 368, a voltage spike 380 appears at input signal 352 but it fails to affect output signal 356 because the duration of the spike 380 is not long enough. At time 369, a noise pulse 382 appears at input signal 352 and it also fails to affect the output signal 356 because it does not have enough voltage amplitude.

[0037] The timing diagram 350 shown in **Figure 3B** illustrates an example of a comparator (as shown in **Figure 10** below), which employs a hysteresis offset for reducing the effect of small-amplitude noise and uses a hysteresis delay for reducing the effect of large-amplitude pulses of insufficient duration.

[0038] **Figure 4** is a schematic diagram of a comparator 400 illustrating an implementation of a hysteresis offset in accordance with one embodiment of the present invention. Comparator 400 includes a comparing circuit 450, two n-transistors N3, N4, a resistor R3, and a source current S5. A first input terminal In1 is connected to the gate terminal of N3 and a second input terminal In2 is connected to the gate terminal of N4. An N-transistor is referred to as an n-type transistor or N-MOS (metal-oxide-semiconductor) transistor.

[0039] In one embodiment, n-transistors N3 and N4 are similarly sized so that they behave similarly. The source terminals of N3 and N4 are connected to a first reference potential. The first reference potential may be Vdd, positive potential, and/or positive voltage supply. The drain terminal of N3 is coupled to a node, which is also connected with terminal 206 of comparing circuit 450, a first terminal of current source S5 and a first terminal of resistor R3. The drain terminal of N4 is coupled to another node, which is also connected to terminal 208 of comparing circuit 450 and a second terminal of resistor R3. The second terminal of current source S5 is coupled to a second reference potential Vss,

which may be a ground reference potential, a zero volt power supply, and/or negative volt power supply.

[0040] In one aspect, comparing circuit 450 produces a logic zero output signal if the input signals on terminals 206-208 are the same. Comparing circuit 450, however, outputs a logic one output signal if the input signals on terminal 206-208 are different. In order to minimize unwanted change of output signals, a hysteresis offset is employed to reduce the switching due to the glitches, noises or voltage spikes. The use of components resistor R3 and current source S5 provides a hysteresis voltage (V_{hyst}) across the resistor R3, wherein V_{hyst} can be expressed as follows:

$$V_{hyst} = R*I$$

Where R is the resistance value of resistor R3 and I is the current value of current source S5. As such, in one embodiment, the output signal from comparing circuit 450 is not going to switch unless the input signal is greater than V_{hyst}.

[0041] **Figure 5** is a schematic diagram illustrating a comparator 500 employing a hysteresis offset and a hysteresis delay in accordance with one embodiment of the present invention. Referring back to **Figure 5**, comparator 500 includes three p-transistors P1-3, three n-transistors N1, N2, N5, two current sources S1-2, one resistor 404 and one capacitor C. The gate terminals of P1 and P2 are coupled to a first node. The drain terminal of P1 and source terminal of N1 are also coupled to the first node. The drain terminal of P2 and source terminal of N2 are coupled to a second node. A first terminal of capacitor and the gate terminal of P3 are coupled to the second node. The source terminals of P1, P2, and P3 are coupled to a first reference potential or Vdd. The drain terminal of N2 is coupled to a first terminal of resistor 404. The second terminal of resistor 404 is coupled to a third node. The drain terminal of N1 and the first terminal of S1 are coupled to the third node. The drain terminal of P3 and the first terminal of S2 are coupled to a fourth node and the fourth node also provides an output terminal 410. The second terminal

of C is coupled to the source terminal of N5. The drain terminal of N5 and the second terminals of S1-2 are coupled to Vss or ground reference potential.

[0042] In one embodiment, components P1-3 and N1-2 provide a comparing function. To implement an accurate comparing function, P1 and P2 have substantially similar parameters so that both P1 and P2 behave similarly under similar conditions. For the same reason, N1 and N2 are also sized to have similar parameters. In operation, output terminal 410 outputs a signal with logic one ("1") when input signals at the input terminals In1-2 are different. Similarly, output terminal 410 outputs a signal with logic zero ("0") when input signals at the input terminals In1-2 are substantially the same. In one embodiment, resistor 404 and S1-2 are configured to create a hysteresis offset or hysteresis voltage. Capacitor C and N5 are configured to provide a hysteresis delay.

[0043] Referring to **Figure 5**, block 530 behaves substantially the same as block 532 because, as discussed earlier, the components in block 530 have similar parameters as components in block 532. By adding a resistor 404 on the path of block 532, it adds impedance on the path of block 532 and effectively reduces the current flow I_2 through block 532. Comparing with block 532, block 530 contains less impedance on its path and consequently, I_1 in block 530 is greater than I_2 in block 532. As such, a higher input signal at In1 406 is needed to turn on P3. Since P3 determines the output value at the output terminal 410, controlling the value of I_2 becomes important because it drives P3. In one embodiment, S1 is used to control the speed of comparator 500. In another embodiment, S2 is used to control the output value at the output terminal 410. When S2 is dominant, the output value at the output terminal 410 is logic zero and when P3 is dominant, the output signal at the output terminal 410 is logic one.

[0044] Block 402 contains capacitor C and transistor N5, which are designed to provide a hysteresis delay. In one embodiment, transistor N5 is used to turn on or off the capacitor C. In one embodiment, block 402 is configured to apply a load on the 2nd node.

Referring to the layout shown in **Figure 5**, by increasing the load on the 2nd node, it delays switching time for P3. In other words, block 402 controls the switching speed of P3. In general, more loading on the 2nd node, requires a wider pulse for an input signal to be valid. The relationship between bandwidth frequency and hysteresis delay T_{hyst} can be expressed as follows:

$$f_{BW} \leq T_{hyst}/(2\pi) \times \ln [\, 1 - (V_{hyst}/V_{min})]$$

where f_{BW} is the bandwidth frequency, V_{hyst} is hysteresis voltage, V_{min} is the minimal voltage, and T_{hyst} is hysteresis delay.

[0045] Referring back to **Figure 5**, the capacitor C in block 402 is used to apply a load on the 2nd node, which controls the rate of switching for P3. In other words, the loading of capacitance from the capacitor C is directly related to the speed of P3. The capacitor C, in one embodiment, is a MOS capacitor, which is also known as a gate capacitance device. In another embodiment, the capacitor C can be turned on or off by a switching device, such as N5. It should be noted that other methods might be used to provide a hysteresis delay. For example, n-transistor may be sized to achieve a similar function as a capacitor. Also, other types of switches such as invertors and p-transistors might be used to perform a switching function to control the capacitor C.

[0046] **Figure 6** is a block diagram illustrating a hysteresis comparator 600 capable of receiving input signals in response to a programmable hysteresis offset and a programmable hysteresis delay in accordance with one embodiment of the present invention. Comparator 600 includes a comparing circuit 610, a programmable hysteresis offset circuit 502, a programmable hysteresis delay circuit 504, and a programmable output control circuit 506. Comparing circuit 610, for one embodiment, is similar to the comparing circuit illustrated in **Figure 5**. It should be noted that the underlying concept of the present invention would not change if other types of comparing circuits were used in block 610.

[0047] Referring back to **Figure 6**, the input terminals 406-408 are coupled to the gate terminals of n-transistors N1-2, respectively. Programmable hysteresis offset circuit 502 is coupled to n-transistors N1-2 for providing a hysteresis offset. Programmable output control circuit 506 is coupled to p-transistor P3 for facilitating output signals at the output terminal 410. Programmable hysteresis delay circuit 504 is coupled to the 2nd node for providing a hysteresis delay. Programmable hysteresis offset circuit 502, programmable hysteresis delay circuit 504, and programmable output control circuit 506 are controlled and/or programmed by programmable control signals carried via programmable control terminal 612. In one embodiment, programmable control terminal 612 carries multiple control signals wherein control signals are divided into three portions. The first portion is dedicated to control programmable hysteresis offset circuit 502. The second portion is dedicated to control programmable hysteresis delay circuit 504 and the third portion is dedicated to program programmable output control circuit 506. In another embodiment, programmable control signals are shared between programmable hysteresis offset circuit 502, programmable hysteresis delay circuit 504, and programmable output control circuit 506. The programmable control signals may be provided by a user, a processor, a memory device, and/or a combination of processor and memory devices. It should be noted that memory device may include flash memory, RAM (random-access memory), ROM (read-only memory), and EEPROM (electronically erasable programmable read-only memory).

[0048] Programmable hysteresis offset circuit 502 provides user selectable hysteresis offset for comparator 600. In one embodiment, programmable hysteresis offset circuit 502 includes a resistor and multiple current sources. Depending on the chip standard, a user can select a current source or a combination of current sources to provide a hysteresis offset. The user may make the selection through a processor or a memory device that resides in the system. In another embodiment, programmable hysteresis offset

circuit 502 includes multiple resistors and one current source. Depending on the chip standard, a user may select a resistor or a combination of resistors to provide a hysteresis offset. In yet another embodiment, programmable hysteresis offset circuit 502 includes multiple resistors and multiple current sources. A user can select a pair of resistors and current sources or a combination of resistors and current sources to provide a hysteresis offset. It should be noted that the underlying concept of the present invention would not change if other types of programmable techniques or additional elements were employed in programmable hysteresis offset circuit 502.

[0049] Programmable output control circuit 506, in one embodiment, is configured to selectively provide control of the output signals at the output terminal 410. Due to the various protocols and standards, the output signals, in one embodiment, need to be controlled with respect to the hysteresis offset. A user, in one embodiment, controls programmable output control circuit 506 via the programmable control signal to determine how much P3 needs to be turned on before P3 drives the output signal. Programmable output control circuit 506, in one embodiment, is adjusted together with programmable hysteresis offset circuit 502 to produce a more desirable hysteresis offset. It should be apparent to one skilled in the art that programmable output control circuit 506 can be integrated into programmable hysteresis offset circuit 502.

[0050] Programmable hysteresis delay circuit 504 provides user selectable hysteresis delay T_{hyst} for enhancing noise immunity. Programmable hysteresis delay circuit 504, in one embodiment, includes various capacitors and switchers wherein the switchers are used to selectively turn on and off capacitors. The switchers are controlled by the programmable control signals. Programmable control terminal 612, in one embodiment, includes multiple wires wherein each wire may control a device or a set of devices such as current sources and capacitors. A user may selectively turn on or off a capacitor through a processor or a memory device. It should be noted that the underlying

concept of the present invention would not change if other types of programmable techniques or additional elements were employed in programmable hysteresis delay circuit 504.

[0051] **Figure 7** is a block diagram illustrating a programmable comparator 700 having a resistance component in accordance with one embodiment of the present invention. Comparator 700 includes a comparing circuit 712, a programmable hysteresis offset circuit 702, and a programmable hysteresis delay circuit 504. Programmable hysteresis delay circuit 504, as described earlier, is used to provide a hysteresis delay in response to control signals transmitted by programmable control terminal 708. The control signals transmitted by programmable control terminal 708, in one embodiment, are provided by a user, a processor, and/or memory cells.

[0052] Comparing circuit 712, in one embodiment, includes similar components as comparing circuit 610 shown in **Figure 6**, except an additional resistor 404. Comparing circuit 712 performs a comparing function with a hysteresis offset and a hysteresis delay. Hysteresis offset, in one embodiment, is created through resistor 404 and programmable hysteresis offset circuit 702. Programmable hysteresis offset circuit 702, in one embodiment, includes a programmable current source and a programmable output control current source. The programmable current source is coupled with resistor 404 to furnish hysteresis offset while the programmable output control current source is coupled to P3 to provide control of the output signal. The programmable current source and programmable output control current source are controlled or selected by control signals carried by control terminals 706.

[0053] In one embodiment, the control signals carried by control terminals 706 are used and decoded by both programmable current source and programmable output control current source. In another embodiment, the control signals are divided into two portions wherein a portion of the signals is dedicated to programmable current source while another

portion of the signals is dedicated to programmable output control current source. Control terminals 706 and 708 may be merged into one control terminal. It should be apparent to one skilled in the art that programmable hysteresis offset circuit 702 may contain circuits that perform current source functions. It should be further noted that the underlying concept of the present invention would not change if additional components such as inductance device, capacitance devices, and transistors may be added or removed from comparator 700.

[0054] **Figure 8** is a detailed circuit diagram illustrating a comparator 800 having programmable blocks 810-814 in accordance with one embodiment of the present invention. Block 810 illustrates a device layout of a programmable hysteresis offset circuit. Block 812 illustrates a device layout of a programmable hysteresis delay circuit and block 814 illustrates a device layout of a programmable output control circuit. Control block 850 provides control channels 852-856 for programming block 810-814, respectively.

[0055] Control block 850 may be activated or controlled by signals transmitted through control block terminal 890. In one embodiment, control channels 852 include multiple control wires 860_1-862_x and control channel 854 includes control wires 864_1-866_x, in which x can be any integer numbers. Also, control channel 856 includes control wires 868_1-869_x. Control block 850, in one embodiment, provides control signals in response to the input signals on control block terminal 890. In another embodiment, control block 850 provides control signals through memory cells within control block 850. Various types of volatile and/or non-volatile memory may be used.

[0056] In one embodiment, block 810 includes multiple current sources 820_1-822_x and multiple switchers 824_1-826_x for providing a hysteresis offset. In other words, block 810 can have one current sources or x number of current sources in which x can be a large number. Multiple n-transistors, in this embodiment, are used as switchers 824_1-826_x. A

function of switcher is to switch the current source on or off according to the signals on the control wires. For example, if control wire 860_1 provides a logic high signal, it turns on n-transistor 824_1 and subsequently activates current source 820_1. On the other hand, if control wire 862_x provides a logic low signal, both n-transistor 826_x and current source 822_x are turned off.

[0057] Block 812 includes multiple capacitors 830_1-832_x for providing a hysteresis delay. Block 812 also includes multiple switchers 834_1-836_x that associate with each capacitor for controlling the capacitors. In this embodiment, n-transistors are used as switchers 834_1-836_x to turn on and off capacitors 830_1-832_x. Signals carried by control wires 864_1-866_x control switchers 834_1-836_x wherein switchers 834_1-836_x control capacitors 830_1-832_x. For example, if signals control wires 864_1-866_x are logic low, n-transistors 834_1-836_x are turned off and consequently, capacitors 830_1-832_x are also turned off. In another embodiment, capacitors 830_1-832_x can be turned on or off in any combination. In other words, a user can turn on more than one capacitor at one time.

[0058] Block 814 includes multiple current sources 840_1-842_x with associated switchers 844_1-846_x for controlling output signals at the output terminal 410. Multiple n-transistors are used as switchers 844_1-846_x. A function of the switcher is to switch current source on or off according to the signals at the control wires 868_1-869_x. For example, if control wire 866 provides a logic high signal, it turns on n-transistor 844 and subsequently activates current source 840_1. On the other hand, if control wire 869_x provides a logic low signal, which turns off n-transistor 846_x, current source $842_x$is turned off. It should be noted that the layout in block 810-814 are illustrative and it should be apparent to one skilled in the art that any layout having programmability and perform similar functions might be used in block 810-814.

[0059] **Figure 9** is a schematic diagram illustrating a comparator 900 having detailed programmable circuits 902-906 in accordance with one embodiment of the present

invention. Programmable block 902, in one embodiment, includes four n-transistors B1-B4 as current sources and four n-transistors S1-S4 as switchers. Programmable block 902 is coupled to resistor 404 for providing a hysteresis offset. In one embodiment, n-transistor B1, which is also known as the base or master current source, is turned on all the time because for comparator 900 to work properly, at least one current source needs to be active. Accordingly, the switcher S1 may be removed since current source B1 is not programmable. The current sources B2-B4 are programmable via switchers S2-S4, respectively. In one embodiment, the current source B2-B4 can be programmed or turned on/off in any combination.

[0060] Programmable block 904 includes four n-transistors B5-B8 as current sources and four n-transistors S5-S8 as switchers. Programmable block 904 is configured to control the output signals at the output terminal 410. In one embodiment, n-transistor B5, which is a base current source, is not programmable and accordingly, switcher S5 may be removed. Current sources B6-B8 are programmable via their switchers S6-S8. In one embodiment, current sources B6-B8 can be turned on or off in any combination.

[0061] Programmable block 906, in one embodiment, includes three MOS capacitors C1-C3 and three invertors 910-914 as switchers. Programmable block 906 is coupled to the 2nd node to provide a hysteresis delay. MOS capacitors C1-C3 are also known as gate capacitors because the drain and source terminals of n-transistors C1-C3 are tied together. To turn on the MOS capacitor, the invertor applies a large potential on the opposite site of the gate terminals to create capacitance under the gate. It should be noted that the invertors 910-912 could be alternatively replaced with other types of switches such as n-transistors and/or p-transistors. Capacitors C1-C3 can be turned on independently or in a combination of any three capacitors C1-C3. The control signals at control terminals 920-924 determine which capacitor or capacitors should be activated.

[0062] **Figure 10** is a block diagram illustrating a fixed signal comparing device 1000 for boundary-scan testing in accordance with one embodiment of the present invention. Comparing device 1000 includes two programmable comparators 1002-1004 and one D flip-flop 1006. The output of the D flip-flop 1006 ensures a square waveform (digital information) output. In this embodiment, the output terminal of positive input comparator 1004 is coupled to the set terminal of the D flip-flop 1006 and the output terminal of negative input comparator 1002 is coupled to the clear terminal of the D flip-flop 1006.

[0063] In one embodiment, comparing device 1000 is used as a receiver in a boundary-scan test setting and is capable of providing a digital square waveform output regardless of whether the input signal is DC or AC coupling. Furthermore, because the comparators 1002-1004 are programmable, a user can program the device 1000 according to the required standards under the test.

[0064] **Figure 11** is a flow chart 1100 illustrating a scheme of producing a digital output signal in response to input signals with a hysteresis offset and a hysteresis delay in accordance with one embodiment of the present invention. At block 1104, the process receives first programmable control information, also known as programmable control signal, for selecting a hysteresis offset (or voltage). The first programmable control information, in one embodiment, includes multiple signals representing selecting information. The selecting information may be provided by a user, a processor within the system, and/or a pre-loaded memory device.

[0065] At block 1106, the process programs the first programmable circuit to set hysteresis offset in accordance to the first programmable control information. In one embodiment, every switcher, which could be a transistor, within the first programmable circuit is either set (open) or reset (closed) in response to the information provided by the

first programmable control information. As discussed earlier, switchers control various current sources to implement the hysteresis offset voltage.

[0066] At block 1108, the process receives second programmable control information, also known as programmable control signal, for selecting a hysteresis delay. The second programmable control information, in one embodiment, includes multiple signals representing programming information. The programming information may be provided by a user, a processor within the system, and/or a pre-loaded non-volatile memory device.

[0067] At block 1110, the process programs the second programmable circuit to set hysteresis delay in accordance to the second programmable control information. In one embodiment, every switcher within the second programmable circuit is programmed. In other words, every switcher, which may be a transistor or an invertor, is either set (open) or reset (closed) in response to the information provided by the second programmable control information. As discussed earlier, switchers control various capacitors to create a hysteresis delay.

[0068] At block 1112, the process receives input information from a first and a second input terminal in response to the hysteresis offset and hysteresis delay. The processor will discard any input signal where its voltage amplitude is below the hysteresis offset and/or its pulse is shorter than the hysteresis delay. In one embodiment, the input signals can either be DC coupled or AC coupled. In another embodiment, the process is capable of detecting the voltage differences in millivolts .

[0069] At block 1114, the process produces digital output information in response to the input signals. In one embodiment, the output signal is a digital square waveform regardless of whether the input signals are DC or AC signals.

[0070] In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than restrictive sense.